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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/473,448	12/28/1999	George Thangadurai	042390.P5761	9991

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EXAMINER	
COLEMAN, ERIC	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 12/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/473,448	THANGADURAI ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-19,21-24, and 26-30 (as renumbered)* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-19,21-24, and 26-30 (as renumbered)* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Objection to the claims

1. The copy of the claims filed 10/3/05 contains claims 6,21 and 26 (original). Claims 6,21 and 26 were cancelled in the amendment dated 3/18/02 and therefore the original claims 6,21 and 26 have not been entered. Also the copy of claims do not contain claims 29-31 (currently renumbered as claims 28-30) added in the 3/18/02 amendment. Note the claims are renumbered consecutively including numbering for cancelled and previously presented claims.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4,6-19,21-24,26-30 (as renumbered) are rejected under 35 U.S.C. 103(a) as being unpatentable over Morris (patent No. 5,859,999) in view of Poplingher (patent No. 6,871,275).

3. Morris taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) Means and method for identifying a first logic value stored in a first register (e.g., see col. 1, lines 30-65)[identifying true or false or one or zero in a predicate register];

b) Means and method for branching to a first location within a programming code based upon a first logic value (e.g., see col. 1, line 12-col. 2, line 11)[the logic value of the predicate is used to replace the conditional branch where the branch changes the location in the programming code at which execution takes place and the predicate merely provided the decision on whether to take the branch or not is determined by the predicate logic value instead retrieving data for comparison to determine if the branch would be taken];

c) Means and method for utilizing the first register as a scratch register during execution of the programming code (e.g., see col. 2, lines 12-53)[using the predicate register as a scratch register where the contents of some of the predicated registers is also saved and restored]; and

d) Means and method for restoring the first logic value back to the first register after execution of the programming code has finished (e.g., see col. 1, lines 60-67, and col. 4, lines 30-58).

4. Morris did not expressly detail (claim 1, claim 17 (originally claim 18), claim 21 (originally claim 22) executing the programming code in a processor firmware layer. Miu, however taught this limitation (e.g., see fig. 3 and col. 11, lines 36-68 of Miu) in a system that used scratch registers (e.g., see col. 57, line 26-col. 58, line 29 and col. 79, lines 15-37 and col. 55, line 43-col. 57, line 53 of Miu).

5. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Morris and Miu. One of ordinary skill would have been motivated to incorporate the Miu teachings of control of branching of interrupts using firmware as

taught by Miu at least to ensure the reliability of the control of branching as the microcode would have been stored in a memory that would not lose its data when the system would lose power or was powered down (e.g., see fig. 3, of Miu and col. 11, lines 36-68 of Miu).

6. Morris did not expressly detail (claim 1) that the branching to a location within the programming code based on the first logic value was to a predefined location. Poplingher however taught (e.g., see fig. 1) a branch prediction unit with speculative branch registers in speculative register file (SBR) (e.g., see col. 4, lines 22-41). Each branch register stored branch target and a static prediction ("SP") predetermined by the compiler (e.g., see col. 5, lines 6-23). The logic value of the static prediction was used to determine whether the branch was taken and therefore to determine whether the system branched to a predetermined (target) location in the programming code (e.g., see col. 5, lines 56-67).

7. It would have been obvious to one of ordinary skill in the DP art at the time of the claimed invention to combine the teachings of Morris and Poplingher. Both references were directed to the problems of correctly predicting which location was next location to branch to in when processing programming code. The addition of the Poplingher teachings of providing a predetermined static target prediction would have provided the combined system added quicker processing of the predicate instruction as the target location would have been readily available.

8. As per claim 2, and claim 22 (originally claim 23) Miu taught detecting and occurrence of an interrupt during execution (e.g., see fig. 34 and col. 49, line 54-col. 50, line 11 and col. 51, line 33-col. 52, line 44).

9. As per claim 3, and claim 18 (originally claim 19), claim 23 (originally claim 24) Morris taught identifying a second logic value stored in a second register (e.g., see col. 3, lines 28-33 and col. 1,lines 29-42); branching to a second predefined location within the programming code based upon the second logic value (e.g., see col. 1, lines 29-56, col. 3, lines 19-26); utilizing the second register as a scratch register during execution of the programming code (e.g., see col. 3, lines 34-43); restoring the second logic value back to the second register in response to the second predefined location (e.g., see col. 3, lines 44-64).

10. As per claim 4, (originally claim 5), claim 19 (originally claim 20), claim 24 (originally claim 25) Miu taught the branching to a first predefined location including computer code for identifying the first predefined location from a plurality of predefined locations in the programming code (e.g., see fig.9, and col. 16, lines 3-64).

11. As per claim 6, (originally claim 7), claim 26 (originally claim 27) Miu taught storing programming code in a non-volatile memory (238) (e.g., see fig. 9 and col. 15, lines 9-65).

12. As per claim 7, (originally claim 8), claim 27 (originally claim 28) Miu taught utilizing the first register (scratch register) as an index register during execution of the program code (e.g., see col. 11, lines 62-68). This corresponds to the predicate register this is used as a scratch register in Morris as described above).

13. As per claim 8, (originally claim 9) Morris taught selectively using the predicate registers as predicate registers or scratch registers during execution (e.g., see col. 1, line 29-col. 5, line 5).

14. As per claim 9 (originally claim 10), Morris taught saving states before execution (e.g., see col. 3, lines 34-43) and Miu taught saving the rest of the processor states before execution of interrupt handlers (e.g., see col. 52, line 57-col. 53, line 38).

15. As per claims 28,29,30 (originally respectively claims 29,30,31) Miu taught the processor firmware layer comprises firmware that utilizes machine readable language (e.g., see col. 47, lines 53-63 and col. 55, line 21-col. 56, line 59).

16. Claims 10,12-16(as renumbered) are rejected under 35 U.S.C. 103(a) as being unpatentable over Morris (patent No. 5,859,999) in view of Beckert (patent No. 6,499,078)

17. As per claim 10 (originally claim 11), Morris taught an execution unit (ALU) (e.g., see fig. 1), general purpose registers (102) (e.g., see fig. 1); Memory coupled to the execution unit (Memory in fig. 1); saving architecture state code (e.g., see fig. 2 col. 4, lines 53-65) predefined sections corresponding to a logic value of a register whereby the logic value can be restored in response to the predefined sections (e.g., see col. 4, lines 40-52). Morris did not expressly detail an interrupt handler. Beckert however taught a processor abstraction layer including interrupt handlers (e.g., see col. 1, lines 24-41) that saves architecture state code including plural predefined sections (e.g., see col. 1, lines 24-41)[plural interrupt service routines are stored (or saved in memory for later access) at predefined locations each dedicated to a different interrupt in the

abstraction layer]. Also Beckert taught a logic value (mask value) of a register (mask register) corresponding to a logic value of a register that can be restored in response to processing using the interrupt handler code (e.g., see col. 3, line 60-col. 4, line 58)

18. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Morris and Beckert. Morris taught a data processor with plural devices connected (e.g., see fig..1). Conventional processors provide for processing of interrupts at least to handle competing system processing requirements. Implementing the Morris system with a standard off the shelf systems such as an x86 based microprocessor would have comprised means for handling interrupts. One of ordinary skill would have been motivated to incorporate the Beckert teachings of storing dedicated interrupt routines in an abstraction layer at least to facilitate quick access to specialized interrupt processing routines for processing each different type of interrupt.

19. As per claim 12 (originally claim 13) Morris taught an embodiment wherein the predicate registers comprised multiple bits in width (e.g., see col. 3,lines 28-33) and Beckert taught interrupt registers comprising multiple bits (e.g., see col. 4, lines 3-32).

20. As per claim 13, (originally claim 14), claim 14 (originally claim 15),claim 15 (originally claim 16, claim 16 (originally claim 17) Morris taught the logic value of predicate register can be restored in the register (in one embodiment) and memory location (in another embodiment); the predicated register values were saved in general purpose registers so that embodiment the logic value in the predicate register as well as the value in the general purpose register corresponded to the predefined section of code (e.g., see col. 3, lines 34-55 and col. 4, lines 59-col. 5, line 4).

21. Claim 11 (originally claim 12) are rejected under 35 U.S.C. 103(a) as being unpatentable over Morris and Beckert as applied to claim 10 above, and further in view of Miu (patent No. 4,484,271).

22. As per claim 11 (originally claim 12), Miu taught storing programming code in a non-volatile memory (238) (e.g., see fig. 9 and col. 15, lines 9-65).

23. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Morris and Miu. One of ordinary skill would have been motivated to incorporate the Miu teachings of control of branching of interrupts using firmware as taught by Miu at least to ensure the reliability of the control of branching as the microcode would have been stored in a memory that would not lose its data when the system would lose power or was powered down (e.g., see fig. 3, of Miu and col. 11, lines 36-68 of Miu).

Response to Arguments

Applicant's arguments with respect to claims 1-4,6-19,21-24 and 26-30 (as renumbered) have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Irie (patent No. 6,772,325) disclosed processor architecture and operation for exploiting improved branch control instruction (e.g., see abstract).

Christie (patent No. 6,009,512) disclosed mechanism for forwarding operands on predicated instructions (e.g. see abstract).

Gschwing (patent No. 6,513,109) disclosed a system for implementing execution predicates in a computer processing system (e.g., see abstract).

Dwyer, III (patent No. 6,430,682) disclose a system for reliable branch predications (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER